ABSTRACT OF THE DISCLOSURE

This invention relates to a clock control system including a CPU, a peripheral functional block for the CPU, a frequency multiplication circuit which multiplies the frequency of an input system clock and outputs the multiplied system clock, a plurality of frequency division circuits which divide the frequency of a signal output from the frequency multiplication circuit to generate clocks to be supplied to the CPU and peripheral functional block, and a clock controller which changes the frequency multiplication ratio of the frequency multiplication circuit to 1/N (positive integer) and then changes the frequency division ratio of the frequency division circuit arranged on the input stage of the peripheral functional block to 1/N in order to set the CPU to a low-power consumption mode, and a method of controlling the clock control system.